**PEDDI PRAVALIKA**

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**CAREER OBJECTIVE:**

I am waiting for wonderful opportunity to work in a competitive environment that can challenge and enhance my skills.

**ACADEMICS**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Qualification** | **Name of the Institute** | **University** | **Year of passing** | **Percentage** |
| BTech (ECE) | Sree Chaithanya College of Engineering, Karimnagar. | JNTUH | 2022 | 70 |
| Diploma (ECE) | Jyothishmathi Institute of Technology and Science, Karimnagar. | SBTET | 2019 | 80 |
| SSC | Vivekananda High School, Poodur. | SSC | 2016 | 85 |

**SUMMARY:**

* Trained in **PHYSICAL DESIGN** domain from SUMEDHA IT, HYDERABAD.
* Expertise on CMOS &TCL Shell scripting language.
* Well known about Synthesis flow & PNR design flow.
* Handled synopsis DC-compiler for SYNTHESIS, ICC2 Shell for PNR.
* Expertise on effective SYNTHESIS, FLOOR PLAN, POWER PLAN, PLACEMENT, CTS, ROUTING.

**Project 01:**

Block : **RP\_TOP**

Technology/Layers : 28nm, 9Layers

Tools : Design Compiler for synthesis, Synopsys Icc2 for PNR

Standard Cell Count : 68649

Frequency : 500MHZ

No. of Clocks : 1 Master clock

Macro Cell Count : 6

**Role:**

To perform Synthesis, Floorplan, Power plan, Placement, CTS, Routing.

**Project 02:**

Block : **ALU**

Technology/Layers : 28nm

Tools : Design Compiler for synthesis

Standard Cell Count : 485

No. of Clocks : 3 Master clocks

**STRENGHTHS:**

* Flexible & Responsible.
* Self-Motivated.
* Quick learner.

**DECLARATION:**

I hereby declare that the above mentioned information and particular furnished above are true to the best of my knowledge.

**(PEDDI PRAVALIKA)**